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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,480	09/27/2001	Kaoru Awaka	TI-33253 (032350.B345)	8718

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 10/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,480	AWAKA ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,9,10,12 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 9-10, 18-20* is/are rejected.

7)☒ Claim(s) *3 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 08/14/2006.

2. Claims 1, 3, 9-10, 12, and 18-20 are pending in this application. Claims 1, 10, and 19-20 are independent claims. In Amendment, claims 2, 4-8, 11, and 13-18 are cancelled. This Office Action is made non-final after a RCE filed 08/14/2006.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 9-10, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hansen et al. (U.S. 2003/01110197 A1).

Re claim 1, Hansen et al. disclose in Figure 2 a multiply-accumulate module (e.g. Figure 2 with 212 ACC as accumulator) comprising: a multiply-accumulate core (e.g. Figure 2), wherein multiply-accumulate core (e.g. Figure 2) comprises:

a plurality of Booth encoder cells (e.g. Figure 3 and page 3 right column paragraph 0043);

a plurality of Booth decoder (e.g. 201 Figure 2) cells connected to at least encoder cells (e.g. 303 in Figure 3);

a plurality of Wallace tree cells (e.g. paragraph 0059 and 202-211 in Figure 2) connected to at least one of Booth decoder cells;

wherein multiply-accumulate module includes a plurality of electrical paths which further include at least one critical path (e.g. any path in Figure 2 would be a critical path as reason under 112 rejection above), the at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal travel from an input of multiply-accumulate core to an output of multiply-accumulate core is greater than or equal to a predetermined amount of time and less than a longest amount of time that it takes any other electrical signal to travel from input of multiply-accumulate core signal to travel from input of multiply-accumulate core to output of multiply-accumulate core, wherein predetermined amount of time is less than a longest amount of time (e.g. translate into mathematical term $t_{pre} < t_{cri} < t_{lon}$ wherein t_{pre} is the predetermined time, t_{cri} is the critical time, and t_{lon} is the longest time; t_{cri} is the path to generate the first output, t_{lon} is the path to generate the last output, t_{pre} is any arbitrary number less than t_{cri});

plurality of Booth decoder cells including at least one first Booth decoder cell and at least one of second Booth decoder cell, at least one first Booth decoder cell structurally the same as at least one second Booth decoder cells (e.g. page 3 right column paragraph 0042) except that a width of at least one of a first plurality of transistors of first Booth decoder cell is greater than a width of a corresponding one of a second plurality of

transistors of second Booth decoder cell (e.g. it is impossible to manufacture all transistors with exact same width);

plurality of Wallace tree cells including at least one first Wallace tree cell and at least one second Wallace tree cell, at least one first Wallace tree cell structurally the same as at least one second Wallace tree cell (e.g. 204 and 207 in Figure 2) except that a width of at least one of a first plurality of transistors of first Wallace tree cell is greater than a width of a corresponding one of a second plurality of transistors of second Wallace tree cell (e.g. it is impossible to manufacture all transistors with exact same width);

wherein at least one first Wallace tree cell and at least one first Booth decoder cell are disposed on at least one critical path (e.g. the critical path running through 4-2 add in Figure 2); and

wherein at least one second Wallace tree cell and at least one second Booth decoder cell are disposed on an electrical path not at least one critical path and are not disposed on any of at least one critical path (e.g. the mux would route through at least one Wallace cell).

Re claim 9, Hansen et al. further disclose in Figure 2 at least one second cell is a most significant bit or a least significant bit and at least one first cell is not a most significant bit or a least significant bit (e.g. Figure 3).

Re claim 10, it is a parallel multiplier with limitations cited in claim 1. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 18, it is a parallel multiplier with limitations cited in claim 9. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 19, it is a method claim of claim 1. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 20, it is a method claim of claim 10. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Allowable Subject Matter

5. Claims 3 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed 09/28/2006 have been fully considered but they are not persuasive.

a. The applicant argues in page 12 for all independent claims that the cited reference fails to disclose the limitation "at least one critical path, the at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal travel from an input of multiply-accumulate core to an output of multiply-accumulate core is greater than or equal to a predetermined amount of time and less than a longest amount of time that it takes any other electrical signal to travel from input of multiply-accumulate

core signal to travel from input of multiply-accumulate core to output of multiply-accumulate core, wherein predetermined amount of time is less than a longest amount of time" as cited in the claimed invention.

The examiner respectfully submits that any circuit for performing a multiplication must have at least a critical path wherein the critical path is the longest path in the circuit to produce a result. Thus, the well-known definition of critical path meets the limitation cited above as it is translated into mathematical term as $t_{pre} <= t_{cri} < t_{lon}$ wherein t_{pre} is the predetermined time, t_{cri} is the critical time, and t_{lon} is the longest time; t_{cri} is the path to generate the first output, t_{lon} is the path to generate the last output, t_{pre} is any arbitrary number less than t_{cri}.

b. The applicant argues in page 13 for all independent claims that the cited reference fails to anticipate the limitation "at least one first Booth decoder cell structurally the same as at least one second Booth decoder cells except that a width of at least one of a first plurality of transistors of first Booth decoder cell is greater than a width of a corresponding one of a second plurality of transistors of second Booth decoder cell" and similarly for the Wallace tree cells. In addition, the cited reference fails to disclose a transistor difference in width of nor cells differing in any dependent upon whether they are in a critical path.

The examiner respectfully submits that the limitation "at least one first Booth decoder cell structurally the same as at least one second Booth decoder cells except that a width of at least one of a first plurality of transistors of first Booth

decoder cell is greater than a width of a corresponding one of a second plurality of transistors of second Booth decoder cell" is clearly addressed above wherein the Booth decoder cell are composed structurally the same type of transistors and it is impossible to manufacture all transistor with exactly width. In addition, the claim does not clearly cite all the transistors in the at least critical path would be difference in width compare to the transistors in non-critical path, but rather at least one of the transistor in the at least critical path.

c. The applicant argues in page 14 that the examiner fails to take into account that "the predetermined time" limitation and the first and second width limitations are tied together in this invention. Further, the cited reference fails to disclose a second transistors having the second width in Wallace tree cells or Booth decoder cells "not disposed on any of said at least one critical path".

The examiner respectfully submits that the claim does not clearly define the relationship between the predetermined time and the first and second width of transistors as alleged by the applicant. The claims only define at least one of Wallace tree cells or Booth decoder cells has difference width compare with the at least one of Wallace tree cells or Booth decoder cells. In addition, the applicant said that the application discloses the critical paths would use the wider transistors which are faster but use more power and the non-critical paths would use the narrower transistors which are slower but use less power. In aggregate, this would make the circuit faster and use less power than using same sized transistors

in all paths. These limitations are not seen in the current claim language. Further, there must be a transistor with difference width that is not disposed on any of at least one critical path.

d. The applicant argues in page 15 second paragraph for claims 9 and 18 that the cited reference fails at least one second cell is a most significant bit or a least significant bit and at least one first cell is not a most significant bit or a least significant bit as seen in the claim.

The examiner respectfully submits that the first or second cell must be either one of bit. In another words, the first or second cell must be either the MSB or the LSB. In general, the current claim language is vast which covers many inventions including the cited reference.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

September 28, 2006